EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	15	sigma NEAR1 delta second NEAR2 error feedback	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/11/15 11:31
L2	2	"5124703".pn.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2006/11/15 11:19
L3	2	"5124703".pn. "4"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2006/11/15 11:20
L4	0	"5124703".pn. filter$4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2006/11/15 11:21

EAST Search History

L5	2	"5124703".pn.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2006/11/15 11:23
L6	2	"5124703".pn. noise	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2006/11/15 11:23
L7	0	sigma NEAR1 delta subtract$ NEAR3 second NEAR2 error feedback	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/11/15 11:32
L8	4	sigma NEAR1 delta subtract$ NEAR3 second NEAR2 error	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/11/15 11:36

EAST Search History

L9	8	sigma NEAR1 delta SAME subtract$ NEAR3 second NEAR2 error	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/11/15 11:53
L10	1	sigma NEAR1 delta SAME subtract$ NEAR3 second NEAR2 error filter$4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/11/15 11:52
L11	4426	(341/143,155,144,141).CCLS.	USPAT	OR	OFF	2006/11/15 11:52
L12	92	sigma NEAR1 delta SAME subtract$ NEAR3 second	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/11/15 11:54
L13	16	sigma NEAR1 delta SAME subtract$ NEAR2 second feedback	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/11/15 12:13

EAST Search History

L14	1	"4733219".pn. and filter$4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2006/11/15 12:54
L15	2	"6147634".pn.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2006/11/15 12:55
L16	2	"6147634".pn. voltage	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2006/11/15 12:57
L17	1	"6147634".pn. "72"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2006/11/15 13:02

EAST Search History

L18	2	"6147634".pn. filter$4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2006/11/15 13:19
L19	1	"6147634".pn. "50"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2006/11/15 13:19

Terms used **sigma delta adc error** Found **61** of **192,172**

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1 Methods and tools for systematic analogue design: Arbitrary design of high order noise transfer function for a novel class of reduced-sample-rate sigma-delta-pipeline ADCs

V. Majidzadeh, O. Shoaei

March 2006 **Proceedings of the conference on Design, automation and test in Europe: Proceedings DATE '06**

Publisher: European Design and Automation Association

Full text available: pdf(441.91 KB) Additional Information: full citation, abstract, references

A novel noise transfer function (NTF) for high order reduced-sample-rate sigma-delta-pipeline (SDP) ADCs is presented. The proposed NTF determines the location of the non-zero poles improving the stabilization of the loop and implementing the reduced-sample-rate structure, concurrently. A design methodology based on simulated-annealing-algorithm is developed to design the optimum NTF. To verify the usefulness of the proposed NTF and design procedure, two different modulators are presented. Simul ...

2 A BIST scheme for on-chip ADC and DAC testing

Jiun-Lang Huang, Chee-Kian Ong, Kwang-Ting Cheng

January 2000 **Proceedings of the conference on Design, automation and test in Europe**

Publisher: ACM Press

Full text available: pdf(114.67 KB) Publisher Site Additional Information: full citation, references, citings, index terms

3 Session 4B: high-level design tools for analog circuits: Verification of delta-sigma converters using adaptive regression modeling

Jeongjin Roh, Suresh Seshadri, Jacob A. Abraham

November 2000 **Proceedings of the 2000 IEEE/ACM international conference on Computer-aided design**

Publisher: IEEE Press

Full text available: pdf(116.40 KB) Additional Information: full citation, abstract, references

A new verification technique for ΔΣ analog-to-digital converters (ADC) is proposed. The ADC is partitioned into functional blocks, and adaptive regression models for each partition are constructed using transistor-level simulation data. Non-idealities in circuit behavior are captured by the adaptive regression technique from the collected data. The

algorithms have been implemented in a simulation program ARSIM (Adaptive Regression Simulator), which performs data sampling, model build ...

4 Session 4B: high-level design tools for analog circuits: DAISY: a simulation-based high-level synthesis tool for ΔΣ modulators

K. Francken, P. Vancorenland, G. Gielen

November 2000 **Proceedings of the 2000 IEEE/ACM international conference on Computer-aided design**

Publisher: IEEE Press

Full text available: pdf(240.09 KB) Additional Information: full citation, abstract, references, citings

An integrated tool called DAISY (*D*elta-Sigma *A*nalys*i*s and *Sy*nthesis) is presented for the high-level synthesis of ΔΣ modulators. The approach determines both the optimum modulator topology and the required building block specifications, such that the system specifications -- mainly accuracy and signal bandwidth -- are satisfied at the lowest possible power consumption. A genetic-based differential evolution algorithm is used in combination with a fast dedi ...

5 Poster session 2: An integrated circuit/behavioral simulation framework for continuous-time sigma-delta ADCs

Mohamed El-Nozahi, Yehia Massoud

April 2006 **Proceedings of the 16th ACM Great Lakes symposium on VLSI GLSVLSI '06**

Publisher: ACM Press

Full text available: pdf(228.10 KB) Additional Information: full citation, abstract, references, index terms

Predicting the performance of the EΔEΔ analog to digital converters (ADCs) is a computationally expensive task that can take several days for estimating the performance. In this paper, we propose a new circuit/behavioral simulation framework for accurately estimating the performance of CT-EΔ-ADCs. Our framework is based on newly developed simulation-directed macro-models and associated mapping techniques for accurately modeling and simulating the CT-EΔ-ADC ...

Keywords: macro-modeling, sigma-delta, simulation

6 (Special session) invited talks: mixed signal test: Delta-sigma modulator based mixed-signal BIST architecture for SoC

Chee-Kian Ong, Kwang-Ting (Tim) Cheng, Li-C. Wang

January 2003 **Proceedings of the 2003 conference on Asia South Pacific design automation ASPDAC**

Publisher: ACM Press

Full text available: pdf(280.80 KB) Additional Information: full citation, abstract, references

This paper proposes a mixed-signal Built-In Self-Test (BIST) architecture based on a second-order delta-sigma modulator. This modulator, which incorporates a design-for-testability (DfT) circuitry, is capable of testing/characterizing itself using digital stimulus. This characteristic is attractive for implementing the modulator as an on-chip analog signal analyzer. When applied for mixed-signal BIST, the modulator-based analog signal analyzer is first characterized using digital stimulus. Then ...

7 Low power mixed-signal and digital systems: Behavioral modeling of Opamp gain and dynamic effectsfor power optimization of Delta-Sigma modulators and pipelined ADCs

Anas A. Hamoui, T. Alhajj, M. Taherzadeh-Sani

October 2006 **Proceedings of the 2006 international symposium on Low power electronics and design ISLPED '06**

Publisher: ACM Press
Full text available: pdf(444.95 KB) Additional Information: full citation, abstract, references, index terms

This paper proposes a simple, yet accurate, analytical model forthe effect of opamp gain and dynamics (slew rate and bandwidth)on the transfer function of switched-capacitor (SC) amplifiers andintegrators. Furthermore, it demonstrates the detrimental effects of:a) the nonlinear variation in the opamp dc gain; and b) thefeedforward transmission of the feedback capacitor, on theharmonic distortion and settling behavior of these SC stages.Theseeffects, typically ignored in the behavioral simulation ...

Keywords: analog-to-digital conversion, behavioral modeling, discrete-time systems, sigma-delta (ΔE) modulation, synthesis

8 Testing: An efficient linearity test for on-chip high speed ADC and DAC using loop-back

Ji Hwan (Paul) Chun, Hak-soo Yu, Jacob A. Abraham
April 2004 **Proceedings of the 14th ACM Great Lakes symposium on VLSI**
Publisher: ACM Press
Full text available: pdf(147.21 KB) Additional Information: full citation, abstract, references, index terms

Our method extracts the linearity of on-chip high speed data converters with minimum area overhead. With a loop-back setup in the presence of noise, differential nonlinearities (DNLs) and integral nonlinearities (INLs) of analog-to-digital converters (ADCs) and digital-to-analog converters (DACs) can be extracted by the proposed method. Our approach exploits the fact that the loop-back output distribution due to noise is distorted by nonlinearities of the ADC, but not by those of the DAC. We fir ...

Keywords: ADC, BIST, DAC, linearity, mixed signal test

9 Analogue and mixed-signal design: Double-sampling single-loop sigma-delta modulator topologies for broadband applications

Mohammad Yavari, Omid Shoaei, Angel Rodriguez-Vazquez
March 2006 **Proceedings of the conference on Design, automation and test in Europe: Proceedings DATE '06**
Publisher: European Design and Automation Association
Full text available: pdf(250.76 KB) Additional Information: full citation, abstract, references

This paper presents novel double sampling high order single-loop sigma-delta modulator structures for wideband applications. To alleviate the quantization noise folding into the inband frequency region, two previously reported techniques are used. The DAC sampling paths are implemented with the single capacitor approach and an additional zero is placed at the half of the sampling frequency of the modulator's noise transfer function (NTF). The detrimental effect of this additional zero on both th ...

10 VLSI circuit design: Adaptive digital techniques to suppress quantization noise of ΣΔ analog to digital converters

Bahar Jalali Farahani, Mohammed Ismail
April 2005 **Proceedings of the 15th ACM Great Lakes symposium on VLSI**
Publisher: ACM Press
Full text available: pdf(462.83 KB) Additional Information: full citation, abstract, references, index terms

This paper investigates the application of Active Noise Cancellation (ANC) techniques in improving the performance of sigma delta ADCs. Using a specific technique of ANC, adaptive line enhancer (ALE), quantization noise of sigma delta modulator can be reduced significantly and signal to noise ratio is boosted. Mathematical model of this system in

steady state is presented. Simulation results on different sigma delta ADCs are very promising and show significant improvements in signal to noise rat ...

Keywords: adaptive noise cancellation, sigma delta modulator

11 Efficient and accurate testing of analog-to-digital converters using oscillation-test method

K. Arabi, B. Kaminska

March 1997 **Proceedings of the 1997 European conference on Design and Test**

Publisher: IEEE Computer Society

Full text available: pdf(511.01 KB) Publisher Site Additional Information: full citation, abstract, citings

This paper describes a practical test approach for analog-to-digital converters (ADCs) based on the oscillation-test strategy. The oscillation-test is applied to convert the ADC under test to an oscillator. The oscillation frequencies are able to monitor the ADC conversion rate, differential nonlinearity (DNL) and integral nonlinearity (INL) at each quantization band edge (QBE). Using this method, no analog stimulus should be supplied and therefore the need for a costly precision signal generato ...

Keywords: A/D convertor, ADC conversion rate, ADC testing, analog-to-digital converters, analogue-digital conversion, differential nonlinearity, digital circuitry, integral nonlinearity, oscillation-test method, quantization band edge

12 On the optimum design of regulated cascode operational transconductance amplifiers

Thomas Burger, Qiuting Huang

August 1998 **Proceedings of the 1998 international symposium on Low power electronics and design**

Publisher: ACM Press

Full text available: pdf(710.23 KB) Additional Information: full citation, abstract, references, index terms

An optimal design procedure to achieve minimum power consumption for a given technology and gain bandwidth is presented. Regulated cascode gain enhancement is used to ensure sufficient DC-gain at minimum gate length transistors. To validate the approach five folded cascode OTA's have been implemented, spanning a bias range of 1µA - 10mA, with measured unity-gain bandwidths within 20% of the designed value. For 17 mW at 3 V, a 0.5 µm

13 Session 57: new ideas in analog/RF modeling and simulation: Lookup table based simulation and statistical modeling of Sigma-Delta ADCs

Guo Yu, Peng Li

July 2006 **Proceedings of the 43rd annual conference on Design automation DAC '06**

Publisher: ACM Press

Full text available: pdf(923.83 KB) Additional Information: full citation, abstract, references, index terms

Sigma-Delta (EΔ) ADCs have been widely adopted in data conversion applications due to the good performance. However, oversampling and complex circuit behavior render the simulation of these designs prohibitively time consuming. In this paper, a lookup table (LUT) based modeling technique is presented for efficient analysis of EΔ ADCs. In the proposed approach, various transistor-level circuit non-idealities are systematically characterized at the building-block level and the ...

Keywords: Sigma-Delta, lookup table, statistical modeling

14 A sigma-delta modulation based BIST scheme for mixed-signal circuits
Jiun-Lang Huang, Kwang-Ting Cheng
January 2000 **Proceedings of the 2000 conference on Asia South Pacific design automation**
Publisher: ACM Press
Full text available: pdf(117.31 KB) Additional Information: full citation, references, citings

15 A new algorithm for the design of stable higher order single loop sigma delta analog-to-digital converters
S. R. Kadivar, D. Schmitt-Landsiedel, H. Klar
December 1995 **Proceedings of the 1995 IEEE/ACM international conference on Computer-aided design**
Publisher: IEEE Computer Society
Full text available: pdf(341.91 KB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

Abstract: This paper presents a new algorithm to attain optimized network scaling in single loop, 1 bit Sigma Delta Analog 1d Digital Converters (SD ADC) of order three or more. The algorithm is based on a novel mathematical description of stability and performance criteria of the SD ADC and on the application of nonlinear interactive optimization techniques. The feasibility of the new algorithm has been confirmed in practical implementations. The method brings new insight on the correlation bet ...

Keywords: CAD, SD ADC, analogue-digital conversion, convertors, electronic engineering computing, higher order, network scaling, nonlinear interactive optimization, performance criteria, sigma delta analog-to-digital converters, single loop

16 Metrics, techniques and recent developments in mixed-signal testing
Gordon W. Roberts
January 1997 **Proceedings of the 1996 IEEE/ACM international conference on Computer-aided design**
Publisher: IEEE Computer Society
Full text available: pdf(240.28 KB) Publisher Site Additional Information: full citation, abstract, references, index terms

This paper presents a tutorial on mixed-signal testing. Our focus is on testing the analog portion of the mixed-signal device, as the digital portion is handled in the usual way. We begin by first outlining the role of test in a manufacturing environment, and its impact on product cost and quality. We look at the impact of manufacturing defects on the behavior of digital and analog circuits. Subsequently, we argue that analog circuits require very different test methods than those presently used ...

Keywords: manufacturing defects, manufacturing environment, measurement setups, mixed analogue-digital integrated circuits, mixed-signal testing, product cost, quality

17 Top-down design of a xDSL 14-bit 4MS/s sigma-delta modulator in digital CMOS technology
R. del Rio, J. de la Rosa, F. Medeiro, B. Pérez-Verdú, A. Rodriguez-Vázquez
March 2001 **Proceedings of the conference on Design, automation and test in Europe**
Publisher: IEEE Press

Full text available: pdf(149.63 KB) Additional Information: full citation, references, index terms

18 Analog and mixed signal design: 4GHz continuous-time bandpass delta-sigma modulator for directly high IF A/D conversion

A. A. Mariano, D. Dallet, Y. Deval, J-B. Begueret

August 2006 **Proceedings of the 19th annual symposium on Integrated circuits and systems design SBCCI '06**

Publisher: ACM Press

Full text available: pdf(1.13 MB) Additional Information: full citation, abstract, references, index terms

We present in this article a fourth-order integrated LC bandpass Delta-Sigma modulator for direct conversion of high intermediate frequencies. It is designed in a 0.25 µm BiCMOS SiGe:C process from STMicroelectronics. The modulator is able to direct digitize a 1GHz IF signal in a 20MHz bandwidth. The continuous-time loop filter employs two integrated LC resonators with active Q?enhancement circuits. A multi-feedback architecture is used to achieve higher order noise-shaping, while maintaini ...

Keywords: A/D conversion, bandpass delta-sigma modulator, continuous-time delta-sigma modulator, high order noise-shaping, high-IF sampling, multi-feedback architecture

19 University design contest: A 0.5-V sigma-delta modulator using analog T-switch scheme for the subthreshold leakage suppression

Koichi Ishida, Atit Tamtrakarn, Takayasu Sakurai

January 2006 **Proceedings of the 2006 conference on Asia South Pacific design automation ASP-DAC '06**

Publisher: ACM Press

Full text available: pdf(378.85 KB) Additional Information: full citation, abstract, references

A 0.5-V sigma-delta modulator implemented in a 0.15-µm FD-SOI process with low VTH of 0.1V using analog T-switch (AT-switch) scheme to suppress subthreshold-leakage problems is presented. The scheme is compared with the conventional circuit, which are also fabricated in the same chip. The measurement result demonstrates that the sigma-delta modulator based on AT-switch realizes 6-bit resolution through reducing non-linear leakage effects while the conventional circuit can achieve 4 ...

20 Implementation of a linear histogram BIST for ADCs

F. Azaïs, S. Bernard, Y. Bertrand, M. Renovell

March 2001 **Proceedings of the conference on Design, automation and test in Europe**

Publisher: IEEE Press

Full text available: pdf(476.52 KB) Additional Information: full citation, references, index terms